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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,734	04/13/2001	Masami Shirosaki	50088-057	6428

7590 04/21/2003

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 04/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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09/833,734	04/13/2001	Masami	

EXAMINER
Maldonado, Julio

ART UNIT	PAPER
2823	13

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Commissioner of Patents and Trademarks

See Attachment

Office Action Summary	Application No.	Applicant(s)	
	09/833,734	SHIROSAKI ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-10 and 12-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-10 and 12-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

ATTACHMENT TO COMMUNICATION

1. The following is a correction of action mailed on 02/28/2003 in response to applicants' telephone inquiry

2. The period of response is reset to three months form the mailing date of this office action.

DETAILED ACTION

3. The non-final rejection as set forth in paper No.9 is withdrawn in response to applicants' amendment.

4. A new 103(a) rejection is made as set forth in this Office Action.

5. Applicant's cancellation to claims 5 and 11 is acknowledged.

6. Claims 6-10 and 12-18 are pending in the application.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 7, 9, 10 and 13-18 rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. According to claims 7, 9, 10 and 13-18, the roughened surface of the lower portion comprises amorphous silicon. However, Sandhu et al. (U.S. 6,190, 992 B1) specifies that the phase transition from amorphous silicon to polycrystalline silicon is at 550°C. Furtherstill, the specification (page 14, lines

3-24) states that the roughening of the amorphous silicon layer is conducted at temperatures of at least 590°C. Therefore, the examiner concludes that there is no support in the specification to claim a roughened amorphous silicon layer.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh et al. (U.S. 5,994,181) in view of the applicants admitted prior art in the instant application and DeBoer et al. (U.S. 6,046,093).

In reference to claims 6 and 7, Hsieh et al. (Figs.1-10c) in a related method to form DRAM capacitors teach the steps of forming a contact hole (46) which penetrates an interlayer insulating film (38, 40) formed on a semiconductor substrate (1); forming an electric conductive film (48) on said interlayer insulating film (38, 40) whereby said contact hole (46) is filled to obtain a contact to said substrate (1); forming an insulating film (51) on said electric conductive film (48); patterning by an anisotropic etching said insulating film (51) and said electric conductive (48) film to form a configuration so that a core and the bottom portion of said configuration are formed; forming the configuration (54) on the side of said core and said bottom portion where said configuration (54) is roughened (column 4, lines 50-52); removing said core; forming a dielectric film (60) to cover said configuration storage node comprising the configuration portion and said

bottom portion; and forming a cell plate (62c) on said dielectric film (60), whereby a capacitor constituted by said configuration storage node, said dielectric film (60) and said cell plate (62) is formed (column 3, line 10 – column 5, line 35).

Hsieh et al. fail to teach that the configuration of the lower electrode is cylindrical. However, the prior art (Figs.6 and 7) teaches forming a DRAM capacitor structure in which the lower electrode (5a) is cylindrical (page 2, lines 1-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a cylindrical-shaped lower electrode as taught by the prior art in the DRAM capacitor structure of Hsieh et al., since the selection of such geometry is part of the conventional procedures used to form DRAM capacitors (page 1, lines 14 and 15).

Hsieh et al. in combination with prior art fail to expressly teach roughening the outer wall of the cylindrical storage electrode, wherein said step comprises forming a film comprising amorphous silicon on said core and said bottom portion; roughening an outer surface of said of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching patterning to form a side-wall-like cylindrical portion at the side of said core and said bottom portion.

However, DeBoer et al. (Figs.12-16) in a related method to form DRAM capacitors teach the step of roughening the outer wall of a storage electrode (70a), wherein said step comprises forming a film comprising amorphous silicon on said core and said bottom portion; roughening an outer surface of said of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching patterning to form a side-wall-like cylindrical portion at the side of said core and said

bottom portion (column 4, line 7 – column 5, line 65 and column 7, lines 19-30). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of the DeBoer et al. with the teachings of Hsieh et al. and the prior art to enable the formation of the roughened surface of DeBoer et al. to be formed.

In reference to claims 8-10, the combination of Hsieh et al., the prior art and DeBoer et al. teach wherein the roughening of the outer surface of the amorphous silicon is performed by a heat treatment with the use of silane and the inner wall having a roughened outer wall was originally constituted by amorphous silicon, wherein said heat treatment is preceded by treating the outer surface of said amorphous silicon with hydrofluoric acid (see DeBoer et al., column 4, line 7 – column 5, line 65).

11. Claims 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh et al. ('181) in view of the applicants admitted prior art in the instant application, DeBoer et al. ('093) and Dennison et al. (U.S. 5,061,650).

Hsieh et al. (Figs.1-10c) in a related method to form DRAM capacitors teach the steps of forming a contact hole (46) which penetrates an interlayer insulating film (38, 40) formed on a semiconductor substrate (1); forming an electric conductive film (48) on said interlayer insulating film (38, 40) whereby said contact hole (46) is filled to obtain a contact to said substrate (1); forming an insulating film (51) on said electric conductive film (48); patterning by an anisotropic etching said insulating film (51) and said electric conductive (48) film to form a configuration so that a core and the bottom portion of said configuration are formed; forming the configuration (54) on the side of said core and

said bottom portion where said configuration (54) is roughened (column 4, lines 50-52); removing said core; forming a dielectric film (60) to cover said configuration storage node comprising the configuration portion and said bottom portion; and forming a cell plate (62c) on said dielectric film (60), whereby a capacitor constituted by said configuration storage node, said dielectric film (60) and said cell plate (62) is formed (column 3, line 10 – column 5, line 35).

Hsieh et al. fail to teach that the configuration of the lower electrode is cylindrical. However, the prior art (Figs.6 and 7) teaches forming a DRAM capacitor structure in which the lower electrode (5a) is cylindrical (page 2, lines 1-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a cylindrical-shaped lower electrode as taught by the prior art in the DRAM capacitor structure of Hsieh et al., since the selection of such geometry is part of the conventional procedures used to form DRAM capacitors (page 1, lines 14 and 15).

Hsieh et al. in combination with prior art fail to expressly teach roughening the outer wall of the cylindrical storage electrode, wherein said step comprises forming a film comprising amorphous silicon on said core and said bottom portion; roughening an outer surface of said of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching patterning to form a side-wall-like cylindrical portion at the side of said core and said bottom portion, wherein the roughening of the outer surface of the amorphous silicon is performed by a heat treatment with the use of silane and the inner wall having a roughened outer wall was

originally constituted by amorphous silicon, wherein said heat treatment is preceded by treating the outer surface of said amorphous silicon with hydrofluoric acid.

However, DeBoer et al. (Figs.12-16) in a related method to form DRAM capacitors teach the step of roughening the outer wall of a storage electrode (70a), wherein said step comprises forming a film comprising amorphous silicon on said core and said bottom portion; roughening an outer surface of said of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching patterning to form a side-wall-like cylindrical portion at the side of said core and said bottom portion, wherein the roughening of the outer surface of the amorphous silicon is performed by a heat treatment with the use of silane and the inner wall having a roughened outer wall was originally constituted by amorphous silicon, wherein said heat treatment is preceded by treating the outer surface of said amorphous silicon with hydrofluoric acid (column 4, line 7 – column 5, line 65 and column 7, lines 19-30). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of the DeBoer et al. with the teachings of Hsieh et al. and the prior art to enable the formation of the roughened surface of DeBoer et al. to be formed in the capacitor structure of the Hsieh et al. and DeBoer et al.

The combined teachings of Hsieh et al., the prior art and DeBoer et al. fail to teach forming a dielectric film on said cylindrical storage node comprising said cylindrical portion and said bottom portion within which said core remains. However, Dennison et al. (Fig.19) in a related method to form a stacked capacitor teach forming a

dielectric film (48) on a storage node comprising a sidewall portion (42) and a bottom portion (34) within which a core (38) remains (column 6, lines 18 – 23). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Dennison et al. with the teachings of Hsieh et al., the prior art and DeBoer et al., to enable the core to remain over the bottom portion of the storage node of the capacitor structure.

Response to Arguments

12. Applicant's arguments filed 01/07/2003 have been fully considered but they are not persuasive.

Applicants argue that "...an ultimate semiconductor device with a roughen amorphous silicon layer is not being claimed...". In response to this argument, claim 7 cites "...roughening an outer surface of said amorphous silicon by forming silicon grains in the outer surface...". Therefore, according to claim 7, a roughened amorphous silicon layer is being claimed.

Also, applicants' argue in reference to claim 6 that Hsieh et al. and DeBoer et al do not teach "...the roughening treatment is conducted right after the formation of the film containing silicon constituting the cylindrical portion...". However, claim 6 does not teach such step. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., roughening treatment is conducted right after the formation of the film containing silicon) are not recited in the rejected claim(s). Although the claims are

interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In reference to claim 7, applicants argue, "...DeBoer et al. does not teach or suggest the step of roughening the outer surface at a lower position of the cylindrical portion 6d and near an upper surface of the interlayer insulating film 4...". However, claim 7 does not teach such step. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., roughening the outer surface at a lower position of the cylindrical portion 6d and near an upper surface of the interlayer insulating film 4) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
4/10/03

George Fourson
Primary Examiner